4 Mbit (256K×16/512K×8) Asynchronous XRAM

January 2019

Features

- Asynchronous XRAM Memory
- High speed access time
  - t_{AA} = 10/12 ns
- Low active power
  - I_{CC} = 55 mA at 80 MHz
- Low CMOS standby current
  - I_{SB2} = 20 mA (Typ)
- Operating voltage range: 2.2 V to 3.6 V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Available in 44-pin TSOP II package and 48-ball FBGA package

Selection Guide

Description	Spec	Unit
Maximum access time	10/12	ns
Maximum operating current	75	mA
Maximum CMOS standby current	35	mA

Functional Description

The XRAM is a new memory architecture designed to provide high-density and high-performance RAM at competitive price. The XRAM uses advanced DRAM technology and self-refresh architecture to significantly improve the memory density, performance and also simplify the user interface.

The XM8A25616V33A/XM8A51208V33A XRAM, which is functionally equivalent to asynchronous SRAM, is a high-performance, 4Mbits CMOS memory organized as 256K words by 16 bits and 512K words by 8 bits that supports an asynchronous SRAM interface.

To write to the device, take Chip Enables (CE) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (DQ_0 through DQ_7), is written into the location specified on the address pins (A0 through A17). If Byte High Enable (BHE) is LOW, then data from I/O pins (DQ_8 through DQ_{15}) is written into the location specified on the address pins (A0 through A17). To read from the device, take Chip Enables (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on DQ_0 to DQ_7. If Byte High Enable (BHE) is LOW, then data from memory appears on DQ_8 to DQ_{15}. See the Truth Table on page 6 for a complete description of Read and Write modes.

The input or output pins (DQ_0 through DQ_{15}) are placed in a high impedance state when the device is deselected (CE), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE and WE LOW). A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

Note: Descriptions about BLE and BHE do not apply to XM8A51208V33A XRAM.

Logic Block Diagram

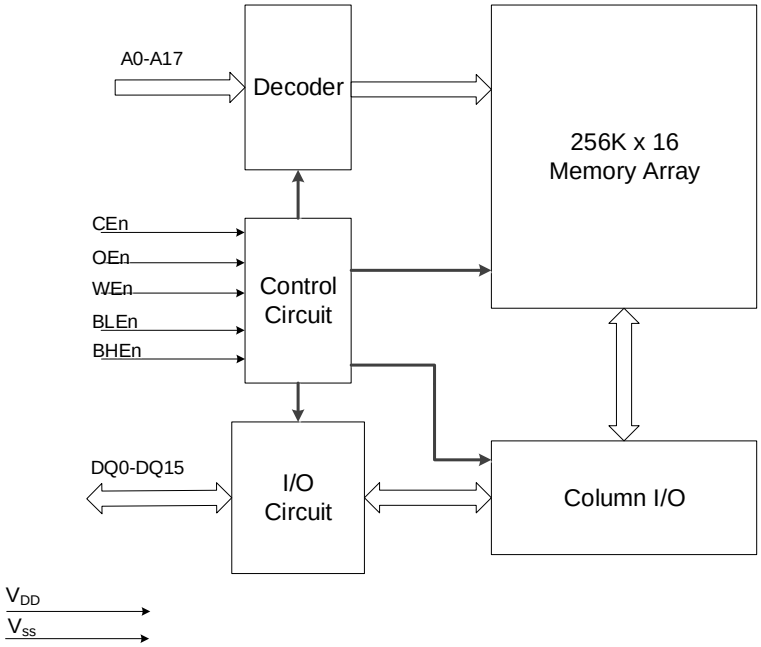


Figure 1 Logic Block Diagram - XM8A25616V33A

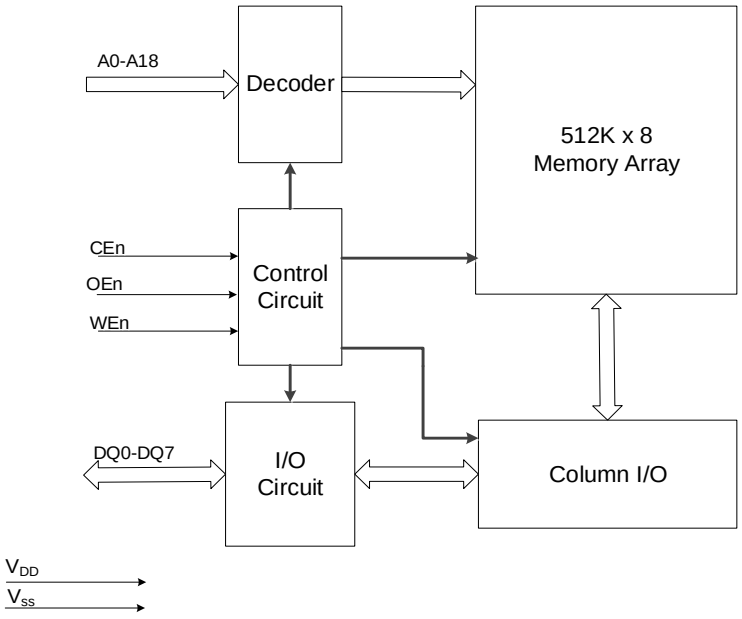


Figure 2 Logic Block Diagram - XM8A51208V33A

Contents

Pin Configurations

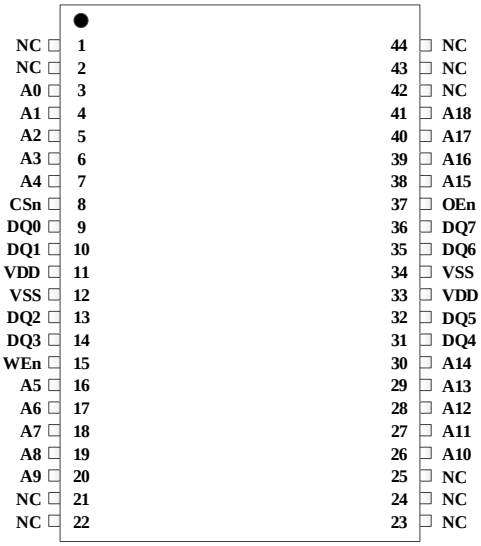


Figure 3 XM8A51208V33A (512K × 8) 44-pin TSOP II pinout

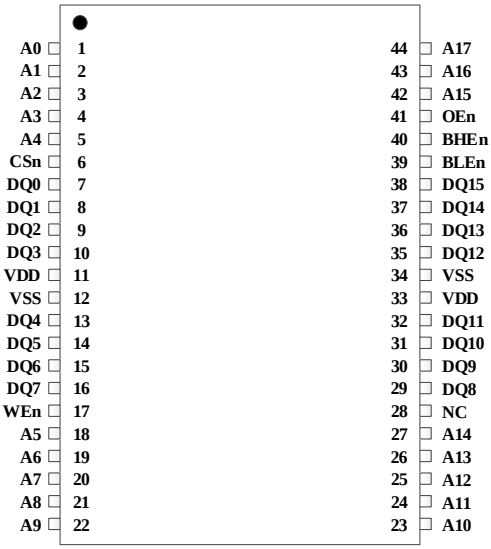


Figure 4 XM8A25616V33A (256K × 16) 44-pin TSOP II pinout

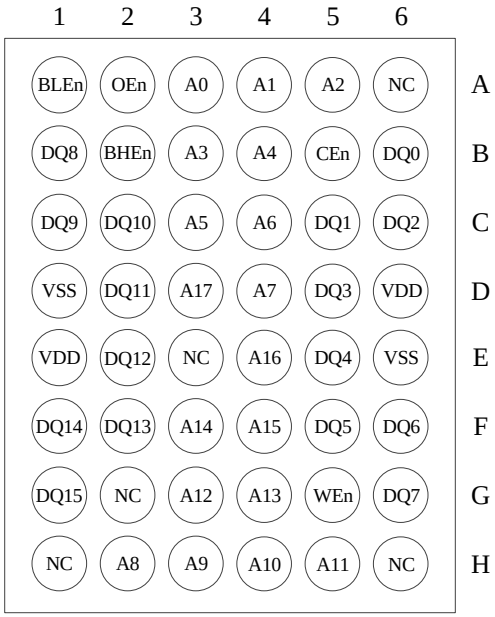


Figure 5 XM8A25616V33A (256K × 16) 48-Ball FBGA Single Chip Enable
Package Code: BG

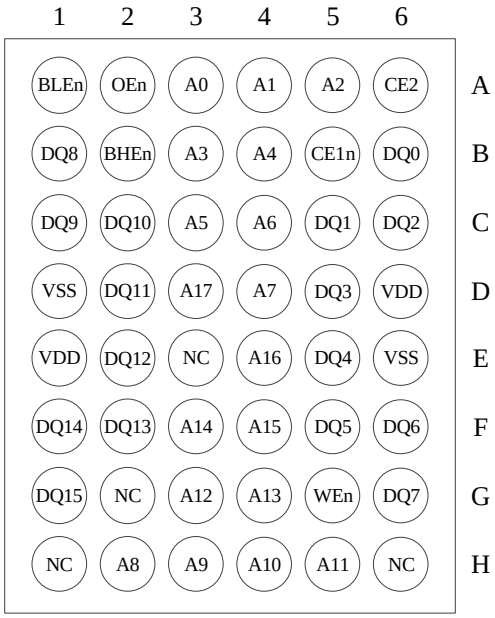


Figure 6 XM8A25616V33A (256K × 16) 48-Ball FBGA Dual Chip Enable
Package Code: B2

Pin Definitions

Name	I/O	Description
V_{DD}	Supply	Power.
V_{SS}	Supply	Ground.
BLEn, BHEn	Input	Byte write enable signal, active LOW.
A0-A18	Input	Address inputs.
CEn, CE1n, CE2	Input	Chip enable signal, active LOW.
OEn	Input	Output enable signal, active LOW.
WEn	Input	Write enable signal, active LOW.
DQ0-DQ15	I/O	Data inputs/outputs.

Note:
For all dual chip enable device, CEn represents the logical combination of CE1n and CE2. When CEn is LOW, CE1n is LOW, CE2 is HIGH. When CEn is HIGH, CE1n is LOW or CE2 is HIGH.

Truth Table

The Truth Table for parts XM8A25616V33A/XM8A51208V33A is as follows*.

Mode	WEn	BLEn	BHEn	CEn	OEn	DQ0-DQ7	DQ8-DQ15
Not Selected	X	X	X	H	X	High-Z	High-Z
Output Disabled	H	X	X	L	H	High-Z	High-Z
Read	H	L	L	L	L	Data Out	Data Out
Read	H	L	H	L	L	High-Z	Data Out
Read	H	H	L	L	L	Data Out	High-Z
Write	L	L	L	L	H	Data In	Data In
Write	L	L	H	L	H	Data In	High-Z
Write	L	H	L	L	H	High-Z	Data In

Note:
Descriptions about BLEn and BHEn do not apply to XM8A51208V33A XRAM.

Maximum Ratings

Item	Description
Storage temperature	–65 °C to + 150 °C
Ambient temperature with power applied	–55 °C to + 125 °C
Supply voltage on V_{DD} relative to GND	–0.5 V to + 4.6 V
DC to outputs in tri-state	–0.5 V to V_{DD} + 0.5 V
DC input voltage	–0.5 V to V_{DD} + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	>4000 V
Latch-up current	>200 mA

Operating Range

Range	Ambient Temperature	V_{DD} (3.3 V - 2.5 V)
Commercial	0 °C to + 70 °C	V_{DD} – 5% / + 10%
Industrial	–40 °C to + 85 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		10/12ns			Unit
				Min	Typ	Max	
V_{OH}	Output HIGH Voltage	for 3.3 V I/O I_{OH} = -4.0 mA		2.4	-	-	V
		for 2.5 V I/O I_{OH} = -1.0 mA		2	-	-	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O I_{OL} = 8.0 mA		-	-	0.4	V
		for 2.5 V I/O I_{OH} = 1.0 mA		-	-	0.4	V
V_{IH}	Input HIGH Voltage	for 3.3 V I/O		2	-	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	for 3.3 V I/O		-0.3	-	0.8	V
		for 2.5 V I/O		-0.3	-	0.7	V
I_X	Input Leakage	GND ≤ V_I ≤ V_{DD}		-5	-	5	µA
	Pull-up Pin	Input = V_{SS}		-30	-	-	µA
		Input = V_{DD}		-	-	5	µA
	Pull-down Pin	Input = V_{SS}		-5	-	-	µA
		Input = V_{DD}		-	-	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DD}, output disabled		-5	-	5	µA
I_{CC}	Operating Supply Current	V_{DD} = Max, IOUT = 0 mA, CMOS levels	f = 100MHz	-	60	75	mA
			f = 83.3MHz	-	55	70	mA
I_{SB1}	Automatic CEn Power-down Current – TTL Inputs	Max V_{DD}, CEn > V_{IH} V_{IN} > V_{IH} or V_{IN} < V_{IL}, f = fMAX		-	-	45	mA
I_{SB2}	Automatic CEn Power-down Current – CMOS Inputs	Max V_{DD}, CEn > V_{DD} – 0.2 V V_{IN} > V_{DD} – 0.2 V or V_{IN} < 0.2 V, f = 0		-	20	35	mA

Capacitance

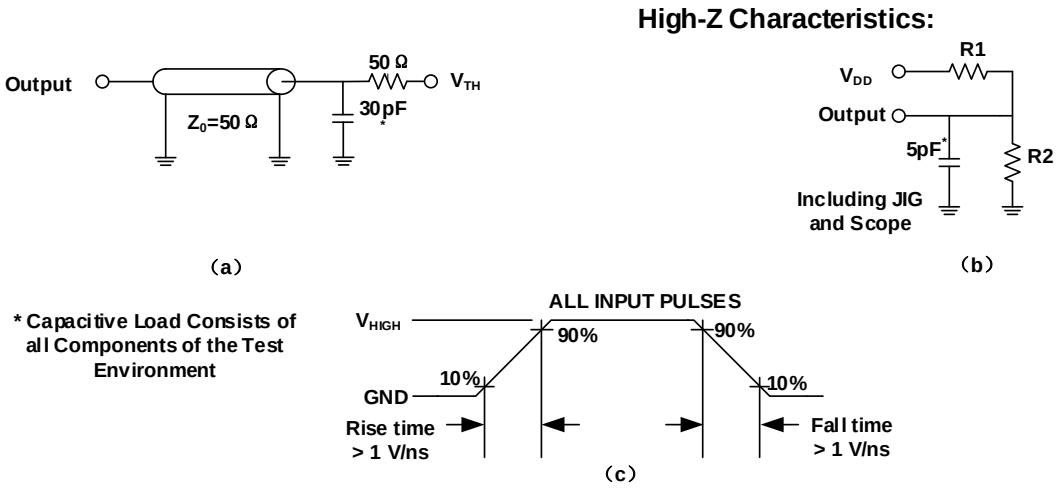
Parameter	Description	Test Conditions	Max*	Unit
$C_{ADDRESS}$	Address input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V	6	pF
C_{DATA}	Data input capacitance		5	pF
C_{CTRL}	Control input capacitance		8	pF
C_{CLK}	Clock input capacitance		6	pF
$C_{I/O}$	Input/output capacitance		5	pF

Note:
These parameters are guaranteed by design and tested by a sample basis only.

Thermal Resistance

Parameter	Description	Test Conditions	TSOP	FBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	TBD	TBD	°C/W
θ_{JC}	Thermal resistance (junction to case)		TBD	TBD	°C/W

AC Test Loads and Waveforms



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Figure 7 AC Test Loads and Waveforms

Switching Characteristics

Over the Operating Range

Parameter	Description	10		12		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{POWER}	V_{DD} to the first access	1000	-	1000	-	μs
t_{RC}	Read cycle time	10	-	12	-	ns
t_{AA}	Address to data valid	-	10	-	12	ns
t_{OHA}	Data hold from address change	9	-	11	-	ns
t_{ACE}	CEn LOW to data valid	-	10	-	12	ns
t_{DOE}	OEn LOW to data valid	-	3.4	-	3.4	ns
t_{LZOE}	OEn LOW to low Z	3.1	-	3.1	-	ns
t_{HZOE}	OEn HIGH to high Z	-	2.3	-	2.3	ns
t_{LZCE}	CEn LOW to low Z	5.5	-	5.5	-	ns
t_{HZCE}	CEn HIGH to high Z	-	5	-	5	ns
t_{PU}	CEn LOW to power-up	-	-	-	-	ns
t_{PD}	CEn HIGH to power-down	-	-	-	-	ns
t_{DBE}	Byte enable to data valid	-	3.6	-	3.6	ns
t_{LZBE}	Byte enable to low Z	3	-	3	-	ns
t_{HZBE}	Byte disable to high Z	-	2.5	-	2.5	ns
Write Cycle						
t_{WC}	Write cycle time	10	-	12	-	ns
t_{SCE}	CEn LOW to write end	7	-	7	-	ns
t_{AW}	Address setup to write end	6.4	-	6.4	-	ns
t_{HA}	Address hold from write end	3.1	-	3.1	-	ns
t_{SA}	Address setup to write start	0	-	0	-	ns
t_{PWE}	WEn pulse width	0.7	-	0.7	-	ns
t_{SD}	Data setup to write end	0	-	0	-	ns
t_{HD}	Data hold from write end	2	-	2	-	ns
t_{LZWE}	WEn HIGH to low Z	5.6	-	5.6	-	ns
t_{HZWE}	WEn LOW to high Z	-	5	-	5	ns
t_{BW}	Byte enable to end of write	0.8	-	0.8	-	ns

Note:

These parameters are guaranteed by design and tested by a sample basis only.

Switching Waveforms

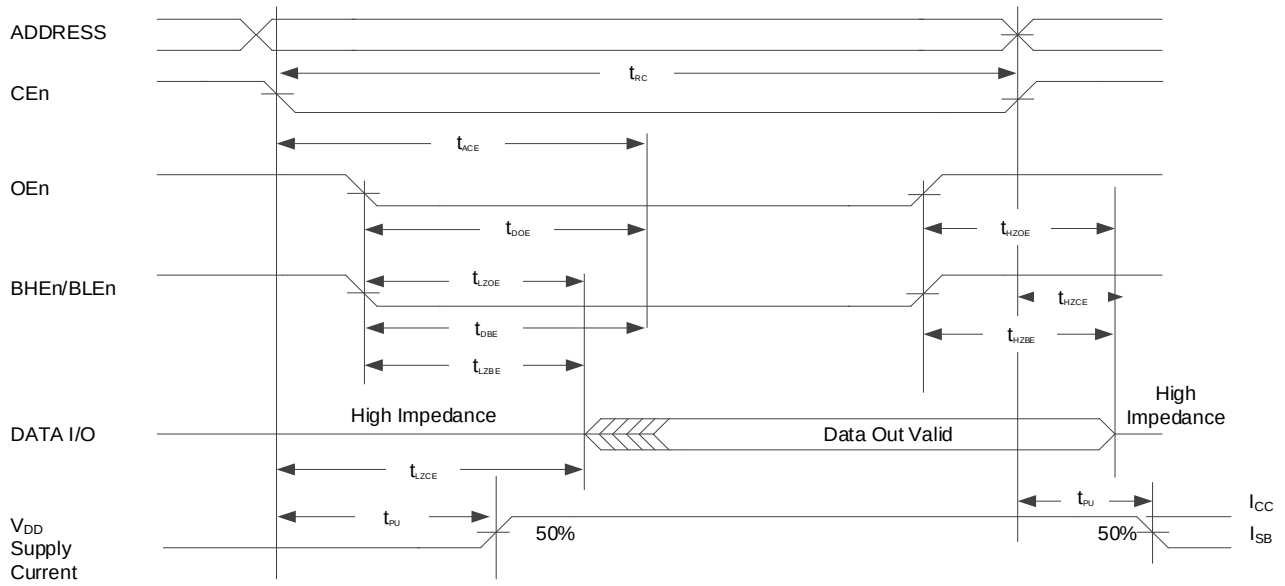


Figure 8 Read Cycle Timing

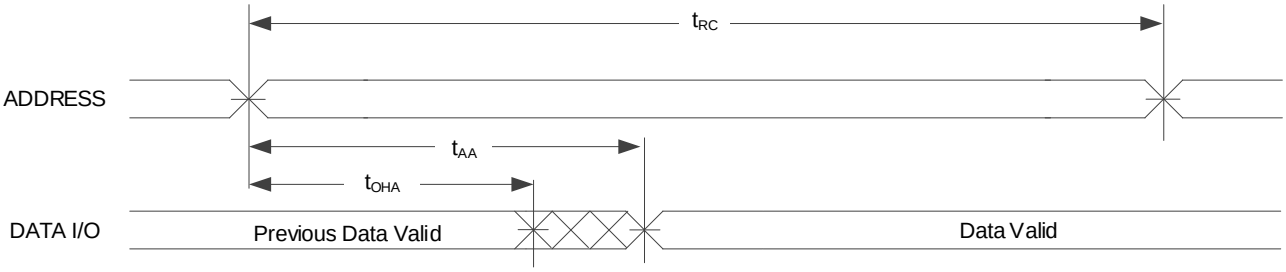


Figure 9 Address Transition Controlled Read Cycle Timing

Notes:

1. The waveform that involves BHEn and BLEn does not apply to XM8A51208V33A XRAM.

2. During the address transition controlled read cycle, CEn is LOW, OEn is LOW, and WEn is in the state of don't care.

Switching Waveforms (continued)

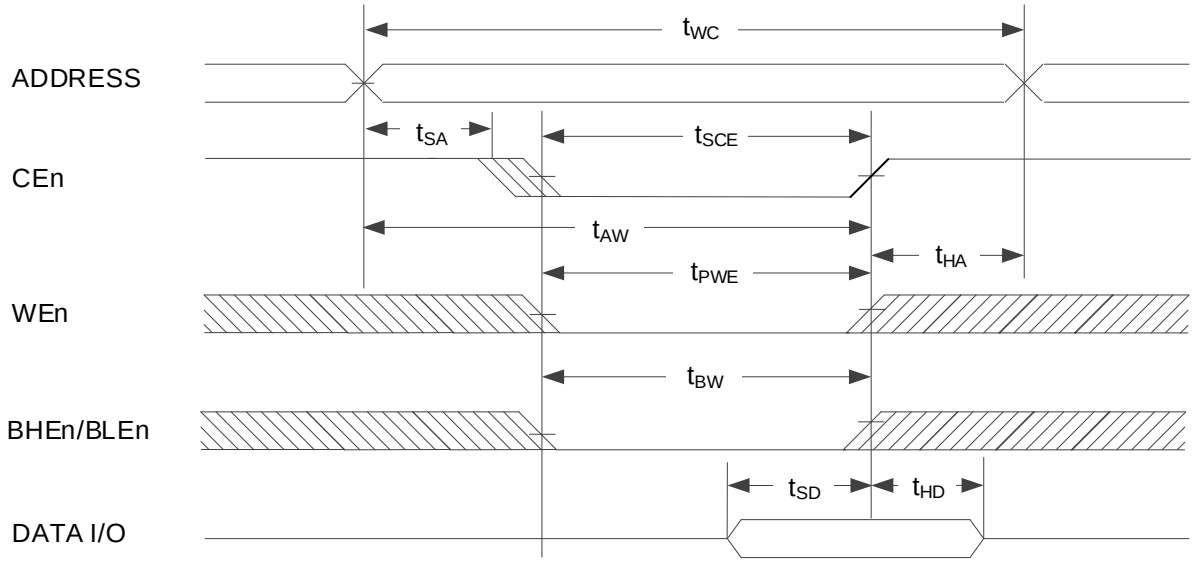


Figure 10 CEn Controlled Write Cycles

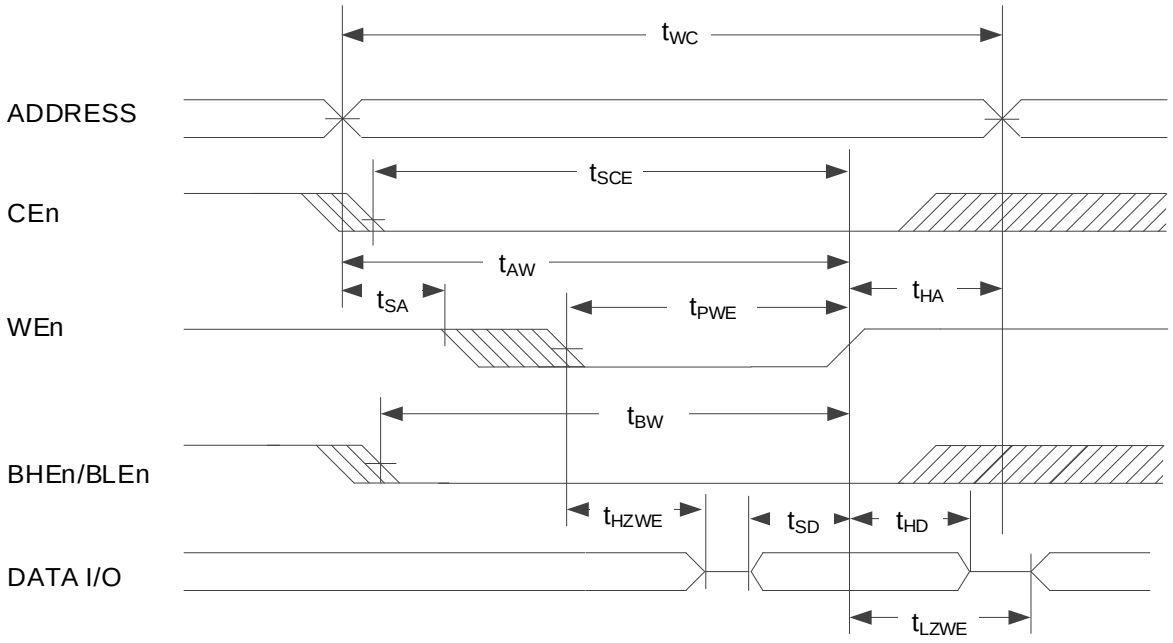


Figure 11 WEn Controlled Write Cycles

Note:

The waveform that involves BHEn and BLEn does not apply to XM8A51208V33A XRAM.

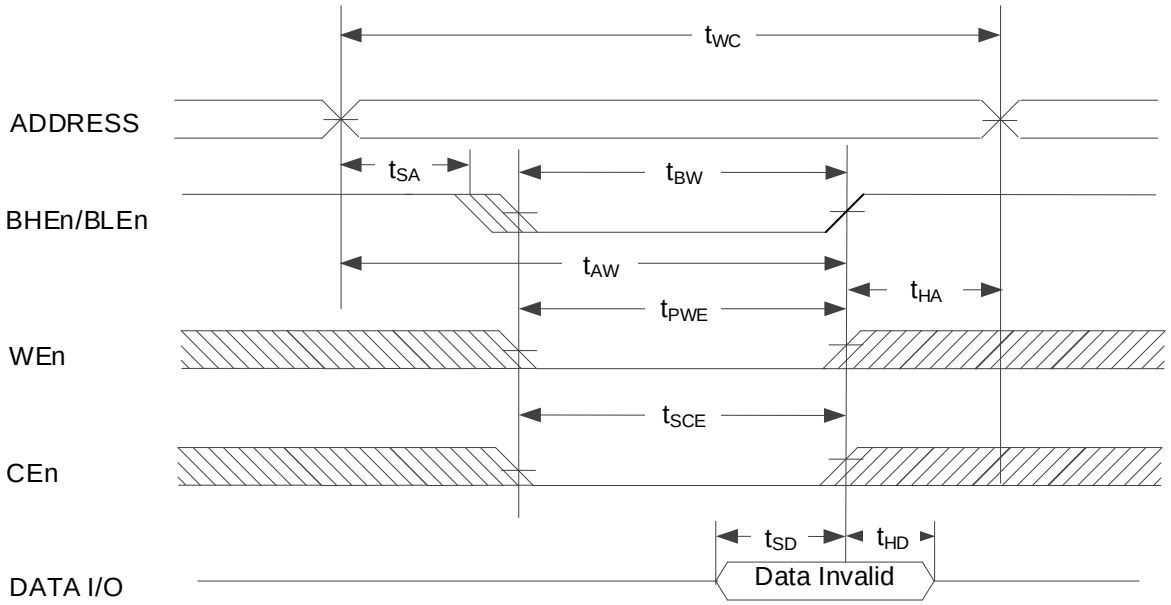


Figure 12 BLEn/BHEn Controlled Write Cycles

Note:

The waveform that involves BHEn and BLEn does not apply to XM8A51208V33A XRAM.

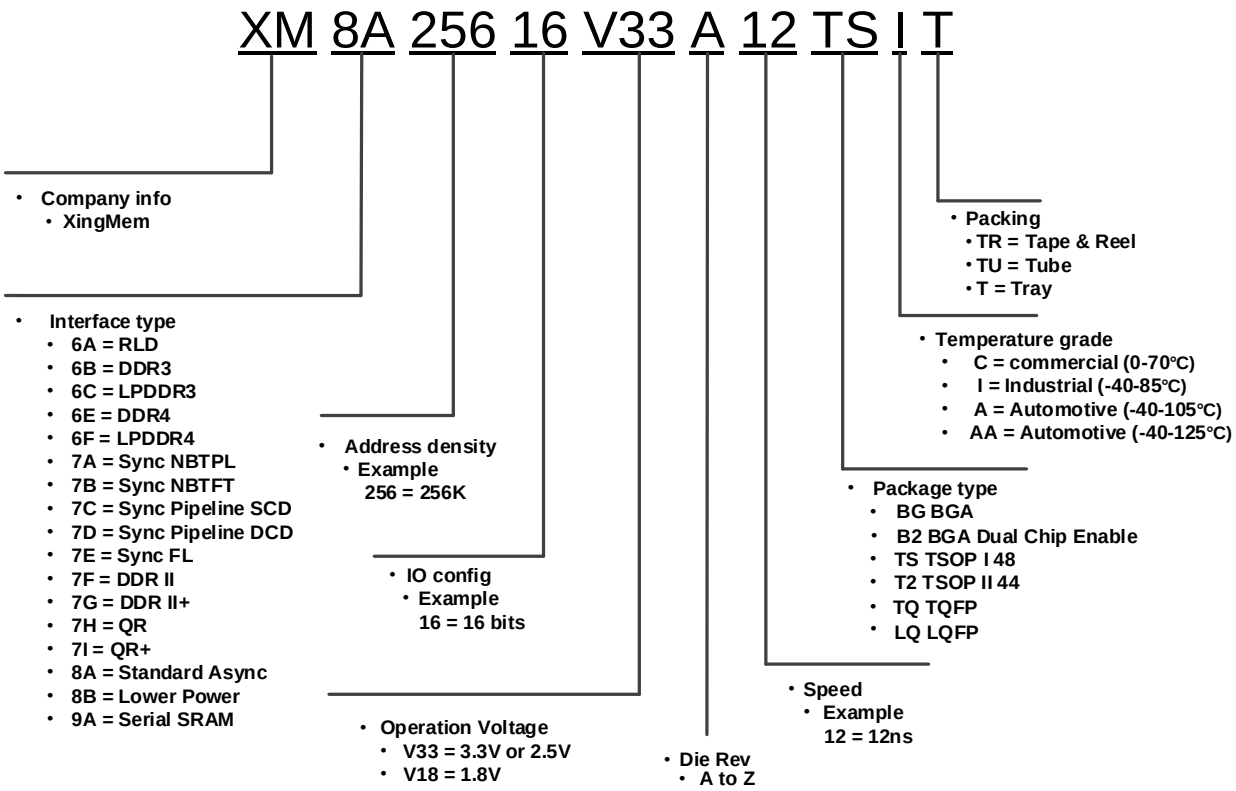
Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative.

Speed (ns)	Ordering Code x 16	Package Type	Operating Range
10	XM8A25616V33A10T2CT	TSOP II 44 (10 × 18.4 × 1.2mm)	Commercial
	XM8A25616V33A10T2IT	TSOP II 44 (10 × 18.4 × 1.2mm)	industrial
	XM8A25616V33A10BGCT	FBGA48 (6 × 8 × 1.2mm)	Commercial
	XM8A25616V33A10BGIT	FBGA48 (6 × 8 × 1.2mm)	industrial
	XM8A25616V33A10B2CT	FBGA48 (6 × 8 × 1.2mm) Dual Chip Enable	Commercial
	XM8A25616V33A10B2IT	FBGA48 (6 × 8 × 1.2mm) Dual Chip Enable	industrial
12	XM8A25616V33A12T2CT	TSOP II 44 (10 × 18.4 × 1.2mm)	Commercial
	XM8A25616V33A12T2IT	TSOP II 44 (10 × 18.4 × 1.2mm)	industrial
	XM8A25616V33A12BGCT	FBGA48 (6 × 8 × 1.2mm)	Commercial
	XM8A25616V33A12BGIT	FBGA48 (6 × 8 × 1.2mm)	industrial
	XM8A25616V33A12B2CT	FBGA48 (6 × 8 × 1.2mm) Dual Chip Enable	Commercial
	XM8A25616V33A12B2IT	FBGA48 (6 × 8 × 1.2mm) Dual Chip Enable	industrial

Speed (ns)	Ordering Code x 8	Package Type	Operating Range
10	XM8A51208V33A10T2CT	TSOP II 44 (10 × 18.4 × 1.2mm)	Commercial
	XM8A51208V33A10T2IT	TSOP II 44 (10 × 18.4 × 1.2mm)	industrial
	XM8A51208V33A10BGCT	FBGA48 (6 × 8 × 1.2mm)	Commercial
	XM8A51208V33A10BGIT	FBGA48 (6 × 8 × 1.2mm)	industrial
12	XM8A51208V33A12T2CT	TSOP II 44 (10 × 18.4 × 1.2mm)	Commercial
	XM8A51208V33A12T2IT	TSOP II 44 (10 × 18.4 × 1.2mm)	industrial
	XM8A51208V33A12BGCT	FBGA48 (6 × 8 × 1.2mm)	Commercial
	XM8A51208V33A12BGIT	FBGA48 (6 × 8 × 1.2mm)	industrial

Ordering Code Definitions

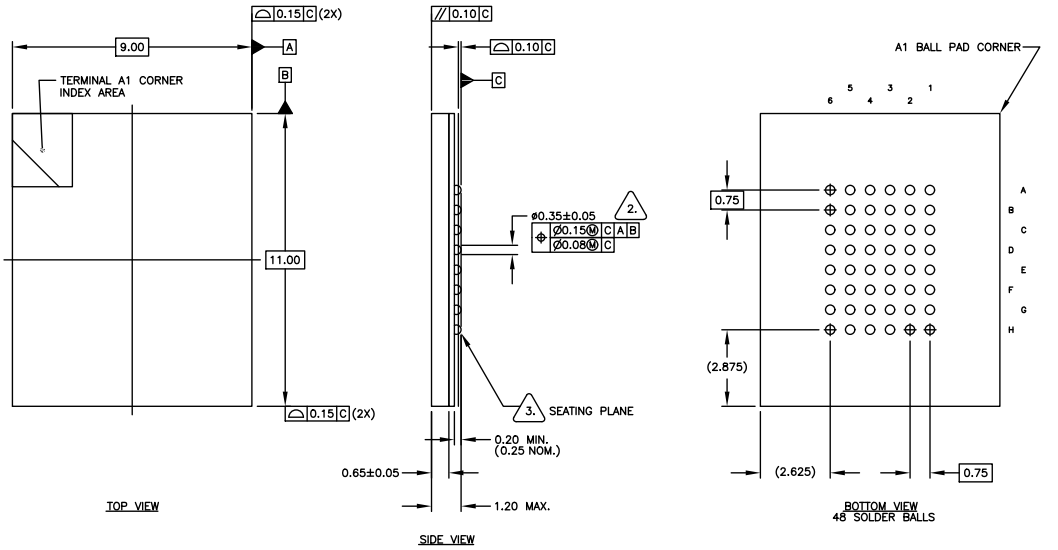


Package Diagrams

SYM.	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30		0.45	11.8		17.7
b1	0.30	0.35	0.40	11.8	14.8	15.7
c	0.12		0.21	4.7		8.3
c1	0.12	0.127	0.16	4.7	5	6.3
E1	9.96	10.16	10.36	392	400	408
e		0.80 BSC			31.5 BSC	
D	18.21	18.41	18.61	717	725	733
E	11.51	11.76	12.01	453	463	473
L	0.40	0.50	0.60	15.7	19.7	23.6
L1		0.80 REF			31.5 REF	
Y			0.075		3	
θ	0°	3°	6°	0°	3°	6°
θ1		15° REF			15° REF	
θ2		15° REF			15° REF	

1.Refer to JEDEC STD. MS-024
2.Dimension D and E1 do not include mold protrusion.
Allowable protrusion is 0.25 mm per side.
D and E1 are maximum plastic body size dimension
include mold mismatch.
3.Dimension b does not include dambar protrusion.
Allowable dambar protrusion shall not cause the lead width
to exceed the maximum b dimension by more than 0.08 mm.
4.All dimensions are in millimeters.

Figure 13 44-pin TSOP II (10 × 18.4 × 1.20 mm) Package Outline



4. REFERENCE SPECIFICATIONS:
   A. AWW SPEC #001–2234: PACKING OPERATION PROCEDURE
   B. AWW SPEC #001–2062: MARKING

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5 – 2009

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 14 48-ball FBGA (6 × 8 × 1.2mm) Package Outline

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CE	Chip Enable
I/O	Input/Output
OE	Output Enable
XRAM	X-Type Random Access Memory
SRAM	Static Random Access Memory
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document Revision History

Date	Version	Changes
Jan 29, 2019	Rev. A1	New datasheet.
April 03, 2019	Rev. A2	Updated Figure 8.