72Mb (2M×36/4M×18) NBT Pipelined XRAM

January 2019

Features

- Pin compatible and functionally equivalent to ZBT/NoBL
  - 100% bus utilization
  - No wait cycles between Read and Write
- Fully registered (inputs and outputs) for pipelined operation
- Internally self-timed Read / Write cycle
- Byte write capability
- Burst capability – linear or interleaved burst order
- Common data inputs and data outputs
- Clock enable (CKEn) pin to suspend operation
- Three chip enables for simple depth expansion
- ZZ sleep mode option and stop clock option
- IEEE 1149.1 JTAG-compatible boundary scan
- Supports 167 MHz bus operation
  - Available speed grades are 167 and 133 MHz
- 3.3V or 2.5V core power supply
- 3.3V or 2.5V I/O power supply
- XM7A02M36V33A/XM7A04M18V33A available in 165-ball FBGA package,100-pin LQFP package

Functional Description

The XRAM is a new memory architecture designed to provide high-density and high-performance memory with competitive price to reduce customer costs. The XRAM uses advanced DRAM technology and self-refresh architecture to significantly improve memory density and performance, and also simplify user interface.

The XM7A02M36V33A and XM7A04M18V33A are 3.3V/2.5V, 2M×36/4M×18 synchronous NBT (No Bus Turnaround) pipelined burst XRAMs with ZBT™ (Zero Bus Turnaround) and NoBL™ (No Bus Latency) logic, respectively. They are designed to provide high performance and high density devices for networking and communication applications. The XM7A02M36V33A and XM7A04M18V33A are equipped with the advanced logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The XM7A02M36V33A and XM7A04M18V33A are pin compatible and functionally equivalent to ZBT/NoBL devices.

All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, or CKEn is HIGH which when deasserted suspends operation and extends the previous clock cycle.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW. Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs when WEn is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

Three synchronous chip enables (CE1n, CE2, CE3n) and an asynchronous output enable (OEn) provide for easy bank selection and output tri-state control. In order to avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

Selection Guide

Description	167MHz	133MHz	Unit
Maximum access time	4.5	4.5	ns
Maximum operating current	240	200	mA
Maximum CMOS standby current	100	100	mA

Logic Block Diagram

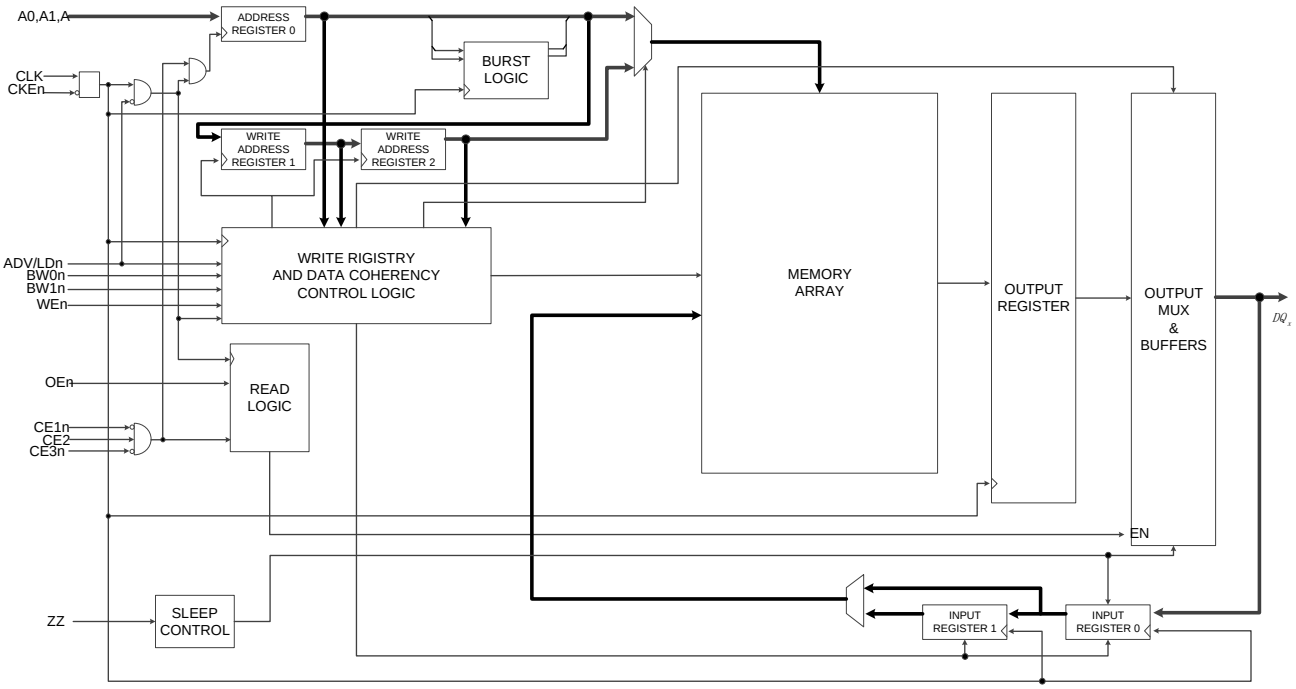

Figure 1 Logic Block Diagram - XM7A04M18V33A/XM7A02M36V33A

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Pin Configurations

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	CE1n	BW1n	NC	CE3n	CKEn	ADV/LDn	A	A	NC
B	NC	A	CE2	NC	BW0n	CLK	WEn	OEn	A	A	NC
C	DQb	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQa
D	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
E	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
F	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
G	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQb	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQb	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQa
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Figure 2 XM7A02M36V33A (2M × 36) 165-ball FBGA (15 × 17 × 1.4 mm) pinout

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	CE1n	NC	NC	CE3n	CKEn	ADV/LDn	A	A	A
B	NC	A	CE2	NC	NC	CLK	WEn	OEn	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQb	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Figure 3 XM7A04M18V33A (4M × 18) 165-ball FBGA (15 × 17 × 1.4 mm) pinout

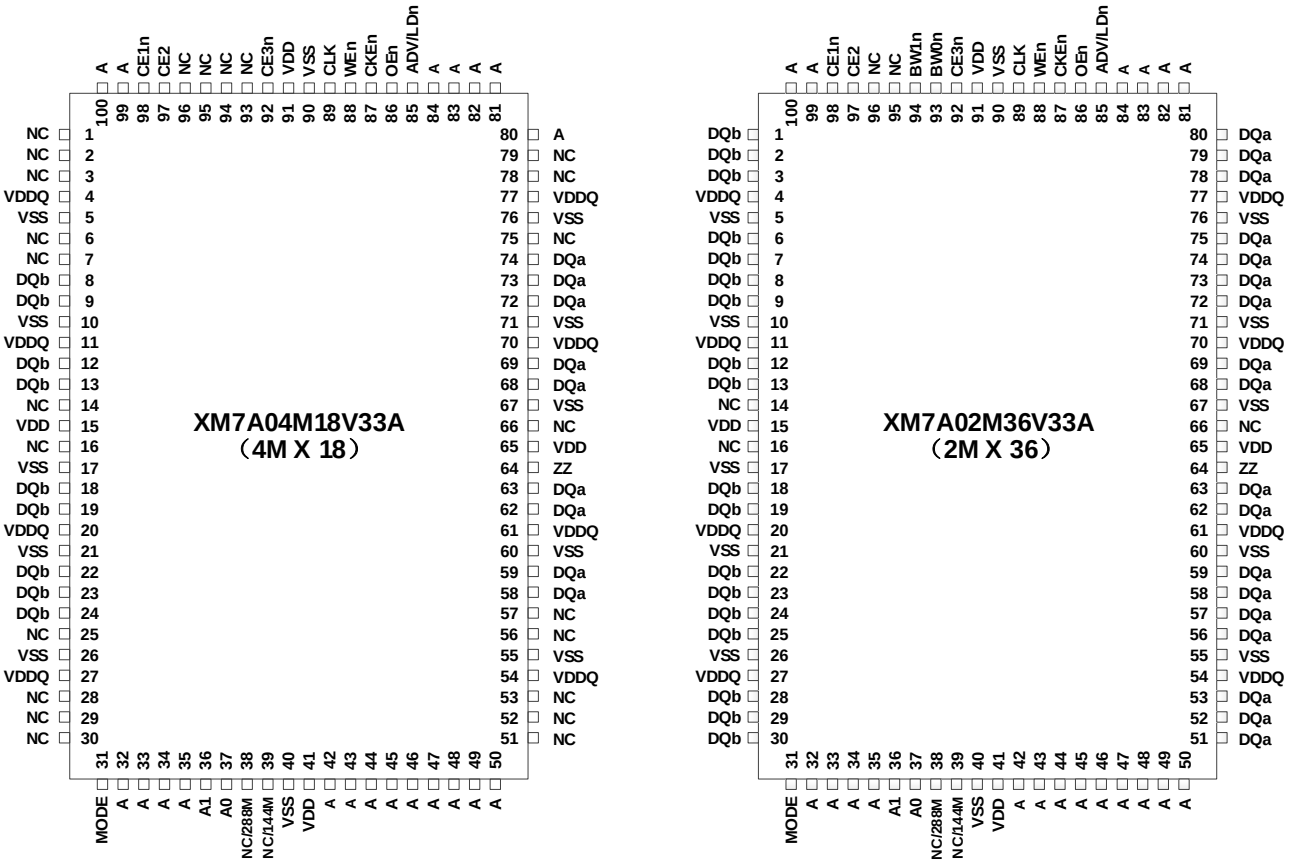


Figure 4 XM7A04M18V33A/ XM7A02M36V33A 100-pin LQFP (14 × 20 × 1.4 mm) pinout

Pin Definitions

Pin Name	I/O Type	Pin Description
CLK	Input	**Clock input**. Used to capture all synchronous inputs to the device. Clock qualified with CKEn is LOW.
CKEn	Input	**Clock enable input**, **active LOW.** When HIGH, the clock signal is masked. Used to extend the previous cycle when required.
CE1n	Input	**Chip enable 1 input**, **active LOW.** Sampled on the rising edge of CLK. Used in conjunction with CE2 and CE3n to select/deselect the device.
CE2	Input	**Chip enable 2 input, active HIGH.** Sampled on the rising edge of CLK. Used in conjunction with CE1n and CE3n to select/deselect the device.
CE3n	Input	**Chip enable 3 input, active LOW.** Sampled on the rising edge of CLK. Used in conjunction with CE1n and CE2 to select/deselect the device.
A,A1,A0	Input	**Address input.** A1, A0 are burst address.
BW1n, BW0n	Input	**Byte write select inputs, active LOW.** BW0n controls DQa; BW1n controls DQb for X36. No Byte mode for X18; BW1n and BW0n are NC.
WEn	Input	**Write enable input, active LOW.** Sampled on the rising edge of the CLK. When LOW, a write sequence is initiated. When HIGH, a read sequence is initiated.
ADV/LDn	Input	**Advance/load address control** When LOW, a new address can be loaded into the device. When HIGH, the internal burst counter is advanced.
MODE	Input	**Mode input.** Selects the burst order of the device. When LOW, a linear burst order is selected. When HIGH, an interleaved burst order is selected. Default leaker to HIGH.
DQb, DQa	I/O	**Bidirectional data I/O** During write cycles, bus data are sampled into data-in registers at the rising edge of the CLK. During read cycles, memory data are sent to the DQ bus. The output enable is controlled by OEn signal.
OEn	Input	**Output enable input, active LOW.** Masked during a write sequence. When LOW, the DQ I/O pins can behave as outputs. When HIGH, the DQ I/O pins are tri-stated, and act as input data pins.
TCK	Input	**JTAG clock input.**
TDI	Input	**JTAG serial data input.** Sampled on the rising edge of TCK.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
TMS	Input	**JTAG mode select input.** Controls the TAP controller state machine. Sampled on the rising edge of TCK.
TDO	Output	**JTAG serial data output.** Delivers data on the negative edge of TCK.
ZZ	Input	**ZZ sleep input, active HIGH.** The input puts device into sleep mode. Default leaker to LOW.
V_{DD}	Supply	**2.5V or 3.3V core power supply.**
V_{DDQ}	Supply	**2.5V or 3.3V IO power supply.**
V_{SS}	Supply	**Ground for the device.**
NC	-	**Not connected to the device.**

Functional Overview

The XM7A02M36V33A and XM7A04M18V33A are synchronous pipelined burst XRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CKEn). If CKEn is HIGH, the clock signal is not recognized and all internal states are maintained. All data outputs pass through output registers controlled by the rising edge of the clock. Operations can be initiated by asserting all three chip enables (CE1n, CE2, CE3n) active at the rising edge of the clock. If clock enable (CKEn) is active LOW and ADV/LDn is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable (WEn). BW1n/BW0n can be used to conduct byte write operations. Write operations are qualified by the write enable (WEn). All writes are simplified with on-chip synchronous self-timed write circuitry. Three synchronous chip enables (CE1n, CE2, CE3n) and an asynchronous output enable (OEn) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LDn should be driven LOW after the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CKEn is asserted LOW, (2) CE1n, CE2, CE3n are all asserted active, (3) the write enable input signal WEn is deasserted HIGH, and (4) ADV/LDn is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus provided OEn is active LOW. After the first clock of the read access the output buffers are controlled by OEn and the internal control logic. OEn must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the XRAM is deselected at clock rise by one of the chip enable signals, its output will tri-state following the next clock rise.

Burst Read Accesses

The XM7A02M36V33A and XM7A04M18V33A have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LDn must be driven LOW in order to load a new address into the XRAM. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap around when incremented sufficiently. A HIGH input on ADV/LDn will increment the internal burst counter regardless of the state of chip enables inputs or WEn. WEn is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) CKEn is asserted LOW, (2) CE1n, CE2 and CE3n are all asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address inputs is loaded into the address register. The write signals are latched into the control logic block. On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the OEn input signal. This allows the external logic to present the data on DQa and DQb. In addition, the address for the subsequent access (read/write/deselect) is latched into the address register. On the next clock rising edge, the data presented to DQa and DQb inputs (or a subset for byte write operations) is latched into the device and the write operation is finished.

The byte data (18 I/Os) written during the write operation is controlled by BW1n and BW0n signals for XM7A02M36V33A and XM7A04M18V33A devices. Asserting the write enable input (WE) with the selected byte write select (BW1n/BW0n) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the XM7A02M36V33A and XM7A04M18V33A are common I/O devices, data should not be driven into the device while the outputs are active. The output enable (OEn) can be deasserted HIGH before presenting data to the DQa and DQb inputs. Doing so will tri-state the output drivers. As a safety precaution, DQa and DQb are automatically tri-stated during the data portion of a write cycle, regardless of the state of OEn.

Burst Write Accesses

The XM7A02M36V33 and XM7A04M18V33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LDn must be driven LOW in order to load the initial address.

When ADV/LDn is driven HIGH on the subsequent clock rise, the chip enables (CE1n, CE2, and CE3n) and WEn inputs are ignored and the burst counter is incremented.

The correct BW1n/BW0n inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the XRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep”

mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE1n, CE2 and CE3n must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Truth Table

The Truth Table for parts XM7A02M36V33A/XM7A04M18V33A is as follows.

Operation	Address	CEn	ZZ	ADV /LDn	WEn	BW1n /BW0n	OEn	CKEn	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L-H	Tri-state
Continue deselect cycle	None	X	L	H	X	X	X	L	L-H	Tri-state
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L-H	Data Out
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L-H	Data Out
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L-H	Tri-state
Dummy read (continue burst)	Next	X	L	H	X	L	X	L	L-H	Tri-state
Write cycle (begin burst)	External	L	L	L	L	H	X	L	L-H	Data In
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L-H	Data In
NOP/write abort (begin burst)	None	L	L	L	L	H	X	L	L-H	Tri-state
Write cycle (continue burst)	Next	X	L	H	X	H	X	L	L-H	Tri-state
Stall	Current	X	L	X	X	X	X	H	L-H	-
Sleep mode	None	X	H	X	X	X	X	X	X	Tri-state

IEEE 1149.1 Serial Boundary Scan (JTAG)

The XM7A02M36V33A and XM7A04M18V33A incorporate a serial boundary scan Test Access Port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not include all functions required to be in full compliance with 1149.1. These functions from the IEEE specification are excluded because they place an added delay in the critical speed path of the XRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs.

Disabling the JTAG Feature

The XRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see Instruction Codes). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the XRAM and may be performed while the XRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the XRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the XRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the XRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 75-bit-long register and the x18 configuration also has a 75-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the XRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the XRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this XRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The XRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the XRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the XRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLES Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all XRAM outputs into a high Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the XRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct value of a signal, the XRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (tcs and tch). To ensure that the XRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-
DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

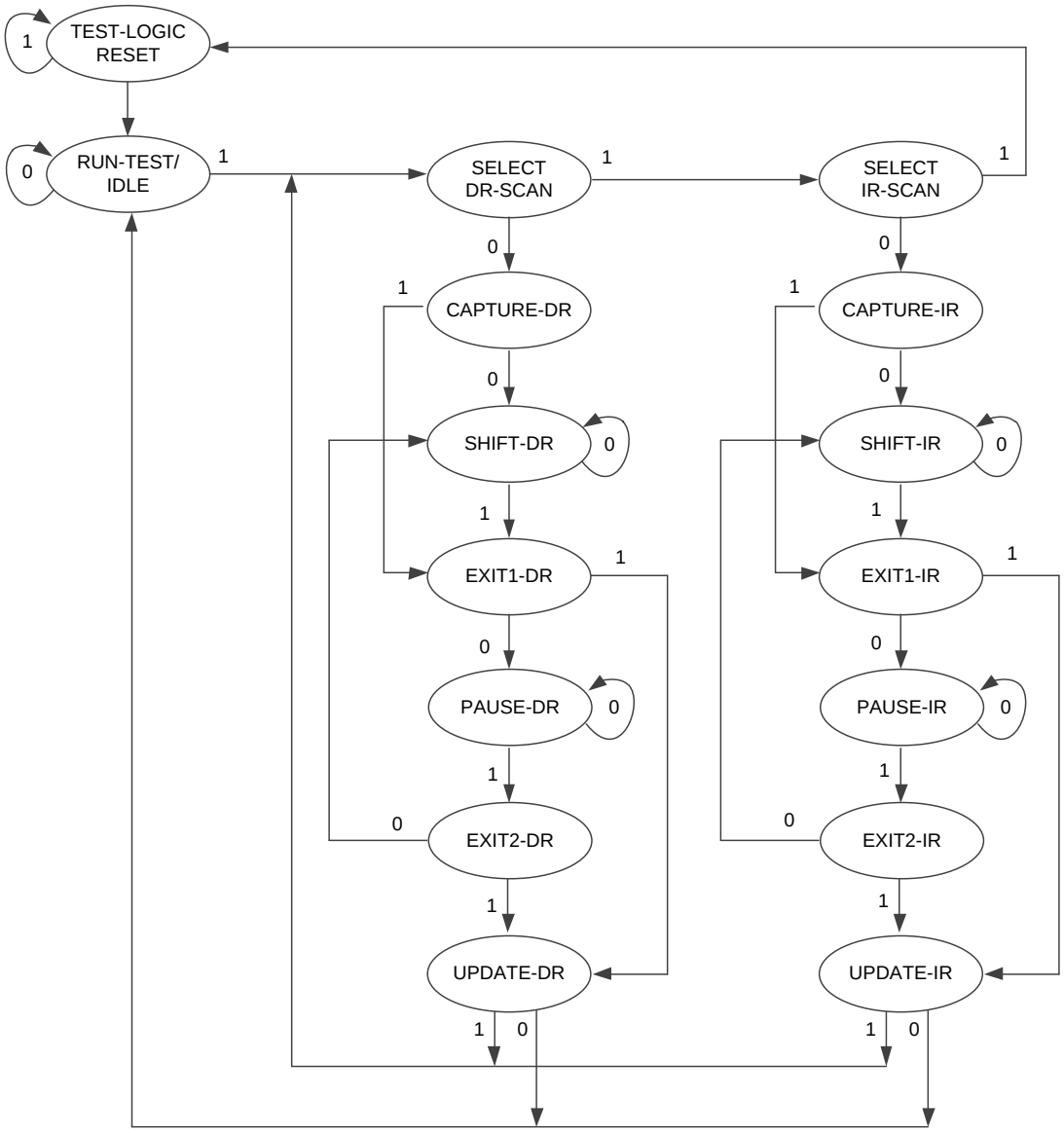


Figure 5 Tap Controller State Diagram

TAP Controller Block Diagram

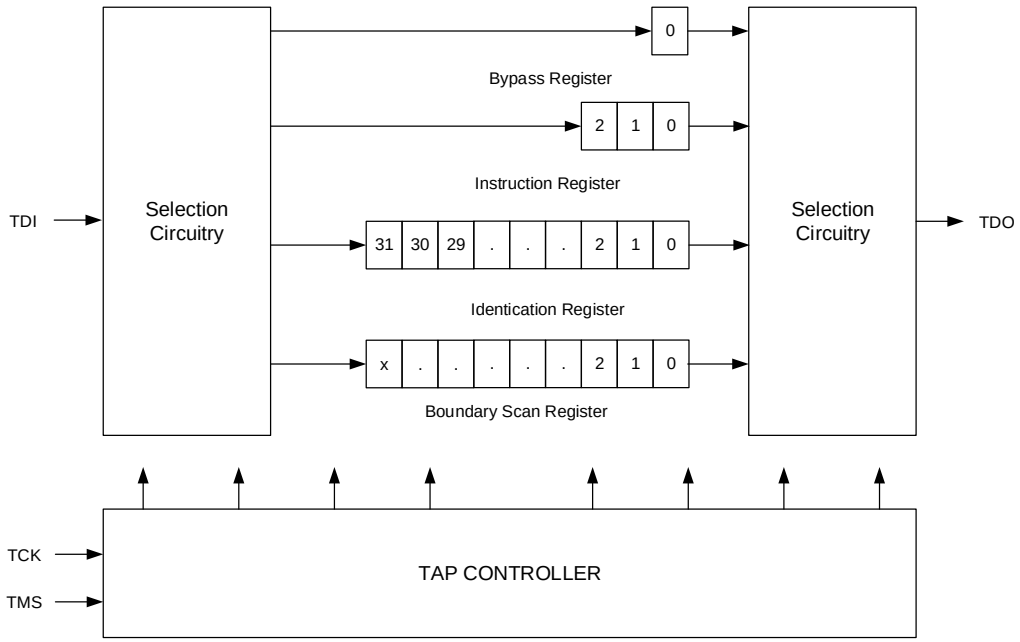


Figure 6 Tap Controller Block Diagram

TAP Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = -4 mA, V_{DDQ} = 3.3V		2.4	–	V
		I_{OH} = -1mA, V_{DDQ} = 2.5V		2.0	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = -100 µA	V_{DDQ} = 3.3V	2.9	–	V
			V_{DDQ} = 2.5V	2.1	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V	–	0.4	V
		I_{OL} = 1 mA	V_{DDQ} = 2.5V	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} =100 µA	V_{DDQ} = 3.3V	–	0.2	V
			V_{DDQ} = 2.5V	–	0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	-0.3	0.8	V
			V_{DDQ} = 2.5V	-0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		-5	5	µA

TAP AC Switching Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
Clock				
t_{CYC}	TCK Clock cycle time	20	-	ns
t_{TF}	TCK Clock frequency	-	50	MHz
t_{TH}	TCK Clock HIGH time	8	-	ns
t_{TL}	TCK Clock LOW time	8	-	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO valid	-	4	ns
t_{TDOX}	TCK Clock LOW to TDO invalid	0	-	ns
Setup Times				
t_{TMSS}	TMS setup to TCK Clock Rise	2	-	ns
t_{TDIS}	TDI setup to TCK Clock Rise	2	-	ns
Hold Times				
t_{TMSH}	TMS hold after TCK Clock Rise	2	-	ns
t_{TDIH}	TDI hold after Clock Rise	2	-	ns

TAP Timing and Test Conditions

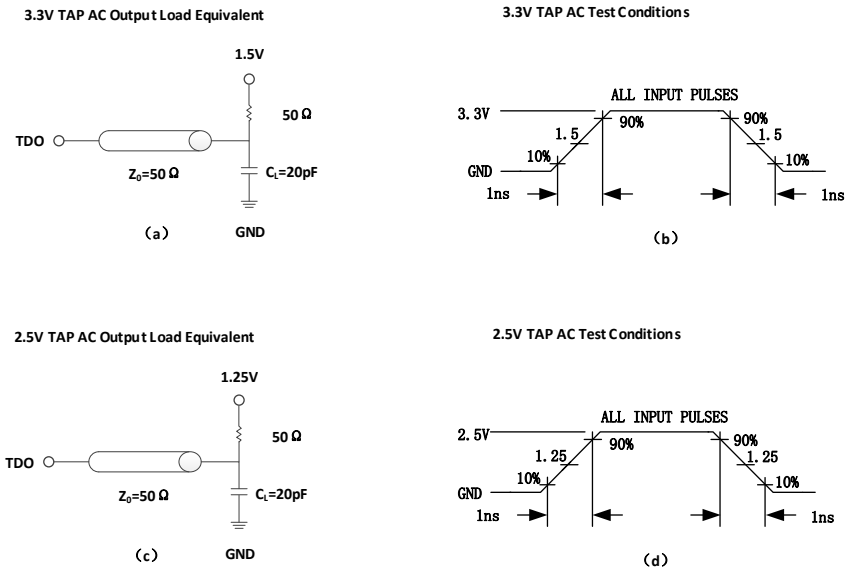


Figure 7 TAP Test Conditions

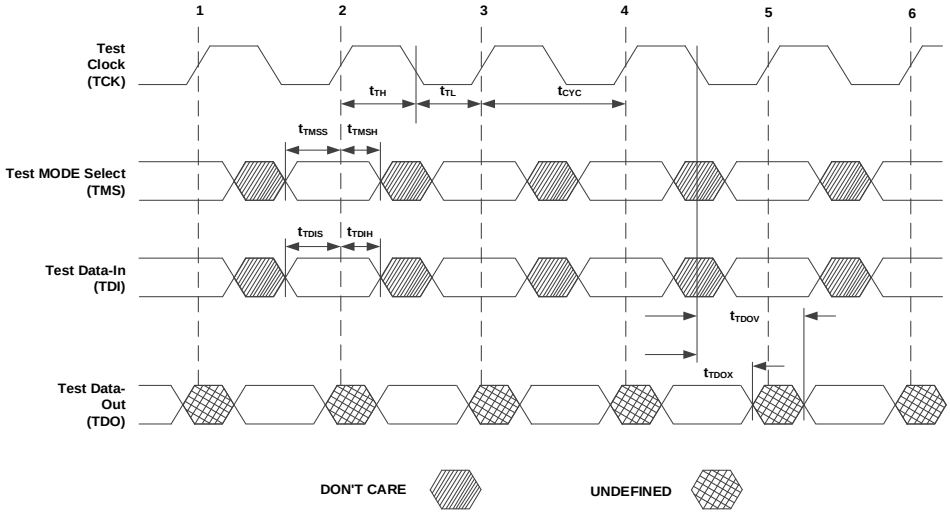


Figure 8 TAP Timing

Identification Register Definitions

Instruction Field	Code (X18)	Code (X36)	Description
Revision Number (31:28)	4'b0000	4'b0000	Describes the version number
Product Type (27:25)	3'b010	3'b010	The product is for sync-XRAM
IO Width Selection (24:19)	6'b000011	6'b000101	IO width
Sub-product Type (18:16)	3'b101	3'b101	Defines memory type and architecture
Address Width (15:13)	3'b100	3'b011	Address width
Byte Mode Select (12)	1'b0	1'b1	1 = Support Byte mode, 0 = Do not support
XM JEDEC ID Code (11:1)	11'b10011000100	11'b10011000100	Enables unique identification of XRAM vendor
ID Register Presence Indicator(0)	1'b1	1'b1	Indicates the presence of an ID register

Scan Register Size

Register Name	Bit Size	
	2M x 36	4M x 18
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary scan	68	51

Instruction Codes

Instruction	Code	Description
EXTEST	3'b000	Captures I/O ring contents.
IDCODE	3'b001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect XRAM operations.
SAMPLE Z	3'b010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all XRAM output drivers to a High Z state.
RESERVED	3'b011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	3'b100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect XRAM operation.
RESERVED	3'b101	Do Not Use: This instruction is reserved for future use.
RESERVED	3'b110	Do Not Use: This instruction is reserved for future use.
BYPASS	3'b111	Places the bypass register between TDI and TDO. This operation does not affect XRAM.

Boundary Scan Exit Order

Bit #	Bump ID (X36)	Bump ID (X18)	Bit #	Bump ID (X36)	Bump ID (X18)	Bit #	Bump ID (X36)	Bump ID (X18)
1	A10	A10	**25**	A7	A7	**49**	L11	NC
2	A9	A9	**26**	H11	H11	**50**	K10	K10
3	B9	B9	**27**	R1	R1	**51**	M11	NC
4	R2	R2	**28**	N1	N1	**52**	L10	L10
5	NC	NC	**29**	M2	NC	**53**	N11	NC
6	NC	NC	**30**	M1	M1	**54**	M10	M10
7	R6	R6	**31**	L2	NC	**55**	D10	NC
8	P6	P6	**32**	L1	L1	**56**	C11	C11
9	P8	P8	**33**	K2	NC	**57**	E10	NC
10	P4	P4	**34**	K1	K1	**58**	D11	D11
11	R8	R8	**35**	J2	NC	**59**	F10	NC
12	R4	R4	**36**	J1	J1	**60**	E11	E11
13	P9	P9	**37**	N11	NC	**61**	G10	NC
14	P3	P3	**38**	M10	M10	**62**	F11	F11
15	R9	R9	**39**	M11	NC	**63**	J11	NC
16	R3	R3	**40**	L10	L10	**64**	A4	A4
17	P10	P10	**41**	L11	NC	**65**	B5	B5
18	B2	B2	**42**	K10	K10	**66**	A3	A3
19	R10	R10	**43**	K11	NC	**67**	B7	B7
20	R11	R11	**44**	J10	J10	**68**	A8	A8
21	NC	A11	**45**	J11	NC	**69**	B3	B3
22	B10	B10	**46**	C11	C11	**70**	A6	A6
23	A2	A2	**47**	D10	NC	**71**	B8	B8
24	B6	B6	**48**	D11	D11			

Maximum Ratings

Item	Description
Storage temperature	–65 °C to + 150 °C
Ambient temperature with power applied	–55 °C to + 125 °C
Supply voltage on V_{DD} relative to GND	–0.5 V to + 4.6 V
Supply voltage on V_{DDQ} relative to GND	–0.5 V to + V_{DD}
DC to outputs in tri-state	–0.5 V to V_{DDQ} + 0.5 V
DC input voltage	–0.5 V to V_{DD} + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	> 2000 V
Latch-up current	> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD} (3.3 V - 2.5 V)	V_{DDQ}
Commercial	0 °C to + 70 °C	V_{DD} – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to + 85 °C		

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage	for 3.3 V V_{DD}		3.135	3.6	V
		for 2.5 V V_{DD}		2.375	2.75	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O I_{OH} = -4.0 mA		2.4	-	V
		for 2.5 V I/O I_{OH} = -1.0 mA		2.0	-	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O I_{OL} = 8.0 mA		-	0.4	V
		for 2.5 V I/O I_{OH} = 1.0 mA		-	0.4	V
V_{IH}	Input HIGH Voltage	for 3.3 V I/O		2.0	V_{DD} + 0.3	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	for 3.3 V I/O		-0.3	0.8	V
		for 2.5 V I/O		-0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		-5	5	µA
	Input Current of MODE	Input = V_{SS}		-90	-	µA
		Input = V_{DD}		-	5	µA
	Input Current of ZZ	Input = V_{SS}		-5	-	µA
		Input = V_{DD}		-	90	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, output disabled		-5	5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0mA, f = f_{MAX} = 1/t_{CYC}	6.0ns cycle, 167MHz	-	240	mA
			7.5ns cycle, 133MHz	-	200	mA

Notes: Power-up: Assumes a linear ramp from 0V to V_{DD} (min) within 200ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Max	Unit
I_{SB1}	Automatic CE Power-down Current-TTL Inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = $1/t_{CYC}$	6.0ns cycle, 167MHz	-	100	mA
			7.5ns cycle, 133MHz	-	100	mA
I_{SB2}	Automatic CE Power-down Current-CMOS Inputs	Max V_{DD}, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ}$ - 0.3 V, f = 0	6.0ns cycle, 167MHz	-	95	mA
			7.5ns cycle, 133MHz	-	95	mA
I_{SB3}	Automatic CE Power-down Current-TTL Inputs	Max V_{DD}, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	6.0ns cycle, 167MHz	-	100	mA
			7.5ns cycle, 133MHz	-	100	mA
I_{SB4}	Automatic CE Power-down Current-CMOS Inputs	Max V_{DD}, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ}$ - 0.3 V, f = f_{MAX} = $1/t_{CYC}$	6.0ns cycle, 167MHz	-	95	mA
			7.5ns cycle, 133MHz	-	95	mA

Notes: Power-up: Assumes a linear ramp from 0V to V_{DD} (min) within 200ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} - 0.2 V	-	120	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} - 0.2 V	-	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	-	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	-	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	-	ns

Capacitance

Parameter	Description	Test Conditions	Max	Unit
$C_{ADDRESS}$	Address input capacitance	TA = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 3.3 V	6	pF
C_{DATA}	Data input capacitance		5	pF
C_{CTRL}	Control input capacitance		8	pF
C_{CLK}	Clock input capacitance		6	pF
$C_{I/O}$	Input/output capacitance		5	pF

Thermal Resistance

Parameter	Description	Test Conditions	165-ball FBGA Package	LQFP 100 Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	23.9	31.5	°C/W
Θ_{JC}	Thermal resistance (junction to case)		5	6.2	°C/W

AC Test Loads and Waveforms

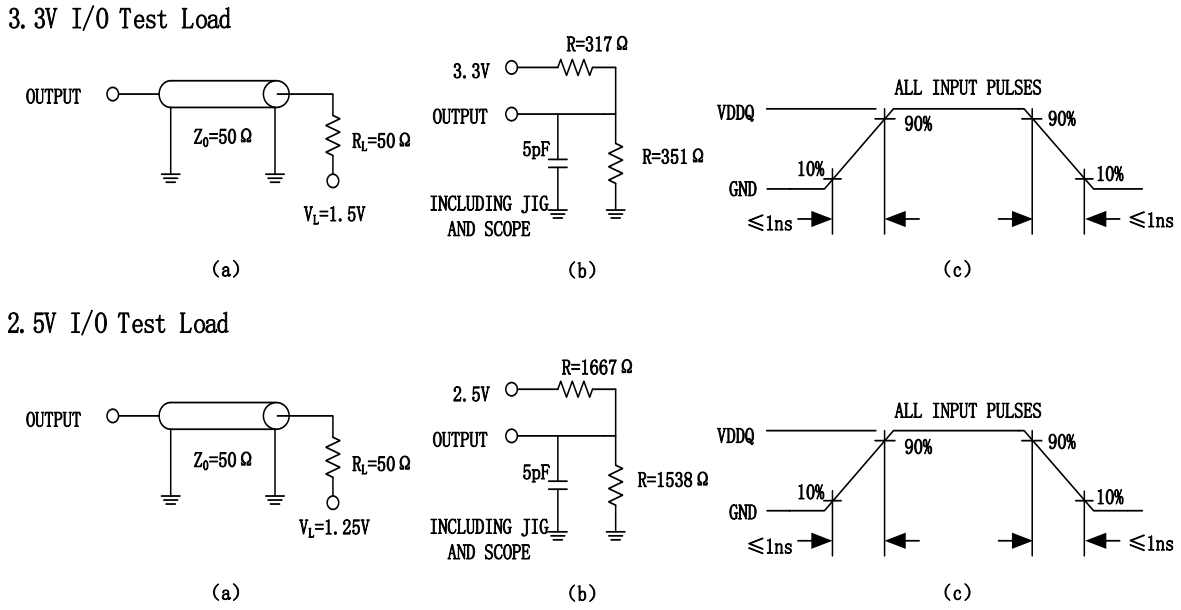


Figure 9 AC Test Loads and Waveforms

Switching Characteristics

Over the Operating Range

Parameter	Description	167MHz		133MHz		Unit
		Min	Max	Min	Max	
t_{Power}	VCC(typical) to the first access Read or Write	1	-	1	-	ms
Clock						
t_{CYC}	Clock cycle time	6	-	7.5	-	ns
F_{MAX}	Maximum operating frequency	-	167	-	133	MHz
t_{CH}	Clock HIGH	2	-	2	-	ns
t_{CL}	Clock LOW	2	-	2	-	ns
Output Times						
t_{CO}	Data output valid after CLK rise	-	4.5	-	4.5	ns
t_{OEV}	OEn LOW to output valid	2.2	-	2.2	-	ns
t_{DOH}	Data output hold after CLK rise	1.7	-	1.7	-	ns
t_{CHZ}	Clock to high Z	-	3.8	-	3.8	ns
t_{CLZ}	Clock to low Z	2.2	-	2.2	-	ns
t_{OELZ}	OEn LOW to output low z		3.2		3.2	ns
t_{OEHZ}	OEn HIGH to output high z	0		0		ns
Setup Times						
t_{AS}	Address setup before CLK rise	0.5	-	0.5	-	ns
t_{DS}	Data input setup before CLK rise	0.5	-	0.5	-	ns
t_{CKENS}	CKEn setup before CLK rise	0.5	-	0.5	-	ns
t_{WES}	WEn, BW_Xn setup before CLK rise	0.5	-	0.5	-	ns
t_{ALS}	ADV/LDn setup before CLK rise	0.5	-	0.5	-	ns
t_{CES}	Chip select setup	0.5	-	0.5	-	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.5	-	0.5	-	ns
t_{DH}	Data input hold after CLK rise	0.5	-	0.5	-	ns
t_{CKENH}	CKEn hold after CLK rise	0.5	-	0.5	-	ns
t_{WEH}	WEn, BW_Xn hold before CLK rise	0.5	-	0.5	-	ns
t_{ALH}	ADV/LDn hold before CLK rise	0.5	-	0.5	-	ns
t_{CEH}	Chip select hold after CLK rise	0.5	-	0.5	-	ns

Notes

Value 3.2 and value 0 are guaranteed by design.

Switching Waveforms

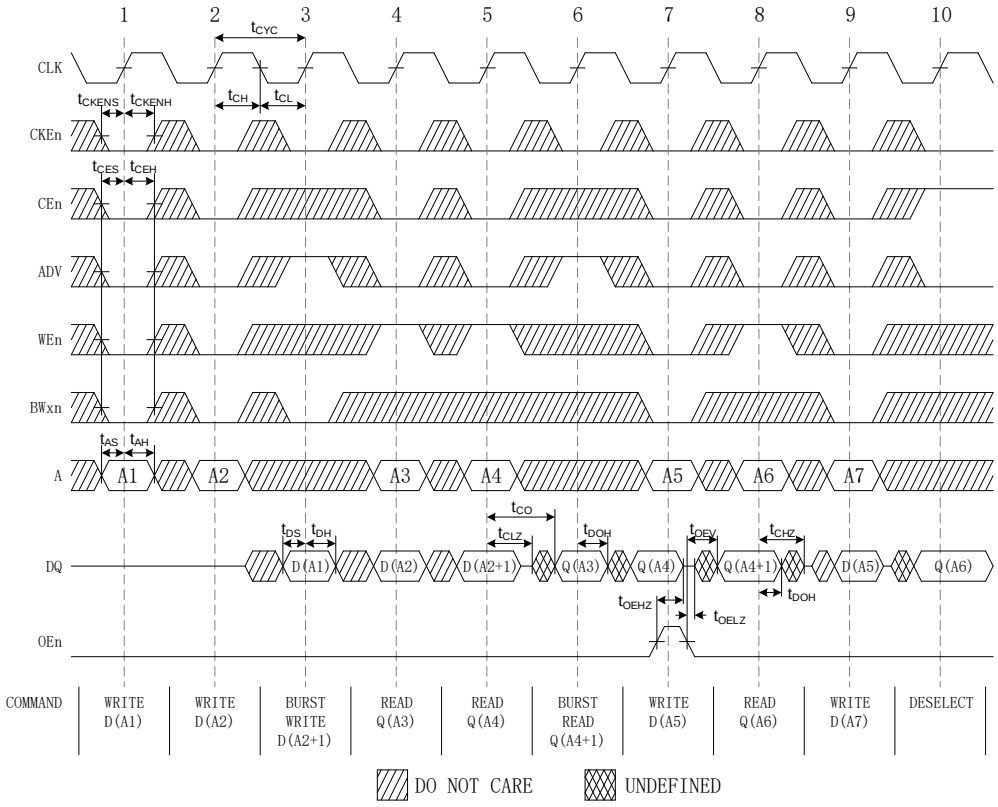


Figure 10 Read and Write Cycle Timing

Notes

When CEn is LOW, CE1n is LOW, CE2 is HIGH and CE3n is LOW. When CEn is HIGH, CE1n is HIGH, or CE2 is LOW or CE3n is HIGH

BWxn indicate BW1n or BW0n or both.

Switching Waveforms (continued)

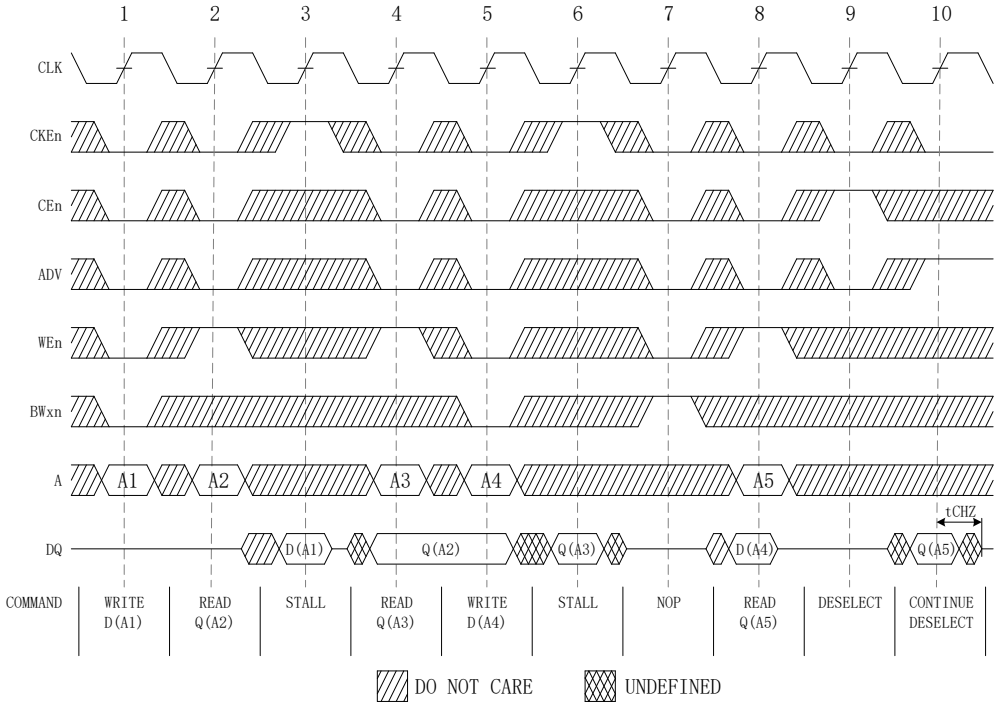


Figure 11 NOP, STALL and DESELECT Cycles

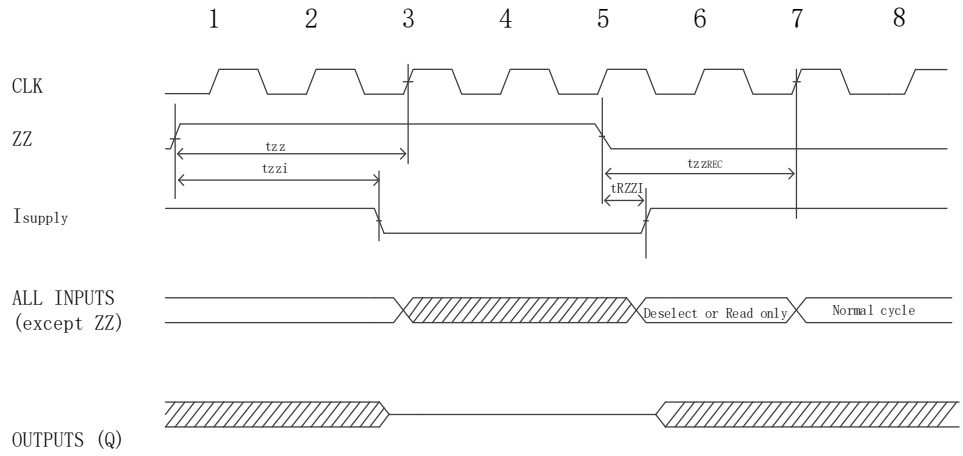


Figure 12 ZZ Mode Timing

Notes

When CEn is LOW, CE1n is LOW, CE2 is HIGH and CE3n is LOW. When CEn is HIGH, CE1n is HIGH, or CE2 is LOW or CE3n is HIGH BWxn indicate 5 or BW0n or both.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representatives.

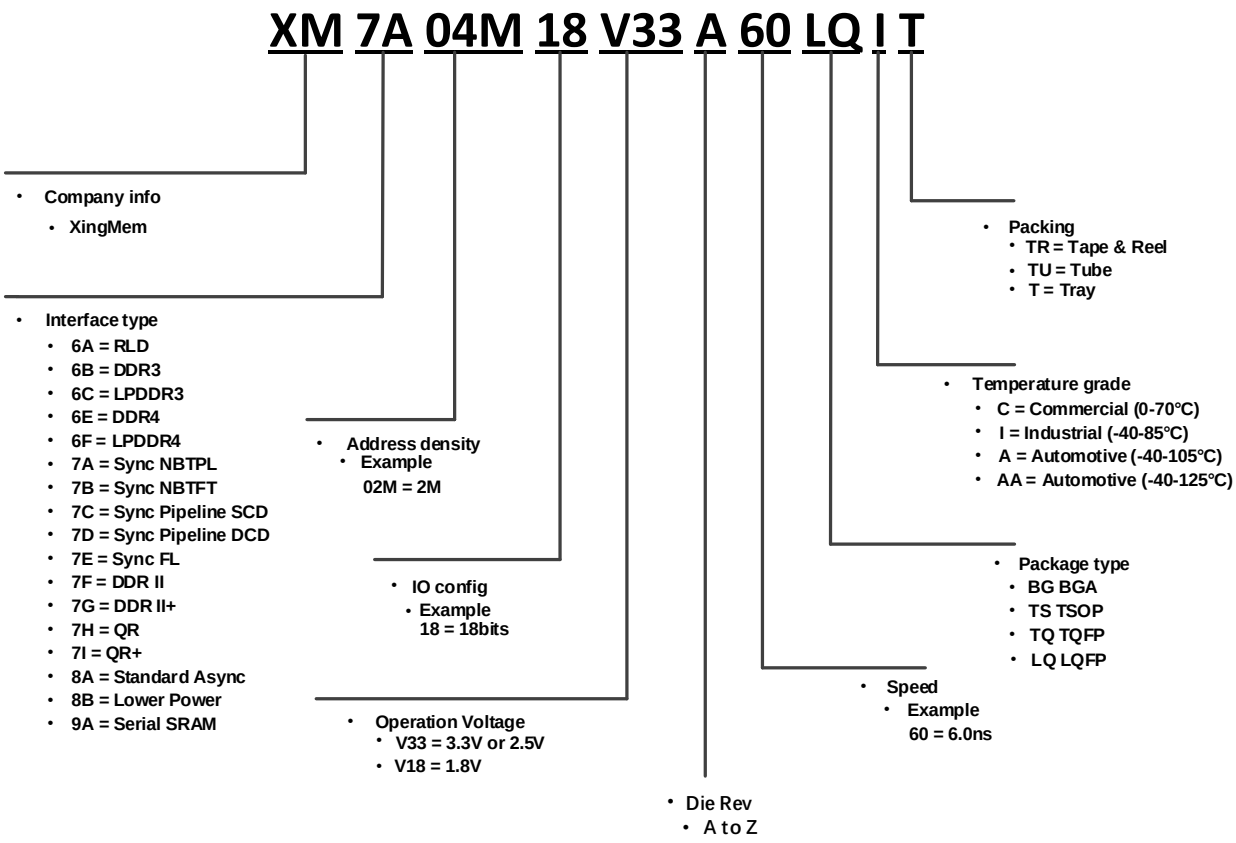
Speed (MHz)	Ordering Code x36	Package Type	Operating Range
167	XM7A02M36V33A60BGCT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Commercial
	XM7A02M36V33A60BGIT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Industrial
133	XM7A02M36V33A75BGCT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Commercial
	XM7A02M36V33A75BGIT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Industrial

Speed (MHz)	Ordering Code x36	Package Type	Operating Range
167	XM7A02M36V33A60LQCT	100-pin LQFP (14 × 20 × 1.4 mm)	Commercial
	XM7A02M36V33A60LQIT	100-pin LQFP (14 × 20 × 1.4 mm)	Industrial
133	XM7A02M36V33A75LQCT	100-pin LQFP (14 × 20 × 1.4 mm)	Commercial
	XM7A02M36V33A75LQIT	100-pin LQFP (14 × 20 × 1.4 mm)	Industrial

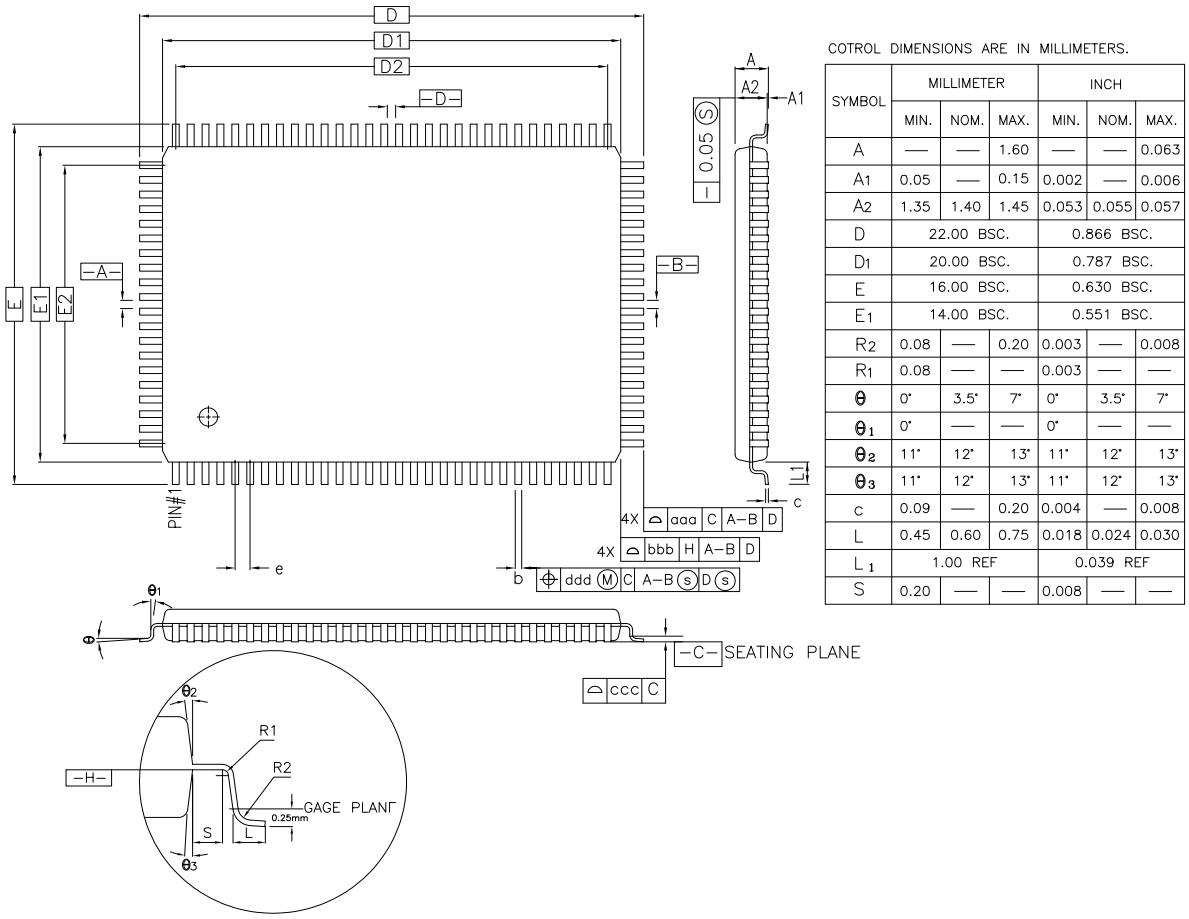
Speed (MHz)	Ordering Code x18	Package Type	Operating Range
167	XM7A04M18V33A60BGCT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Commercial
	XM7A04M18V33A60BGIT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Industrial
133	XM7A04M18V33A75BGCT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Commercial
	XM7A04M18V33A75BGIT	165-ball FBGA (15 × 17 × 1.4mm) Pb-free	Industrial

Speed (MHz)	Ordering Code x18	Package Type	Operating Range
167	XM7A04M18V33A60LQCT	100-pin LQFP (14 × 20 × 1.4 mm)	Commercial
	XM7A04M18V33A60LQIT	100-pin LQFP (14 × 20 × 1.4 mm)	Industrial
133	XM7A04M18V33A75LQCT	100-pin LQFP (14 × 20 × 1.4 mm)	Commercial
	XM7A04M18V33A75LQIT	100-pin LQFP (14 × 20 × 1.4 mm)	Industrial

Ordering Code Definitions



Package Diagrams



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BSC.			0.026 BSC.		
D2	18.85			0.742		
E2	12.35			0.486		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.13			0.005		

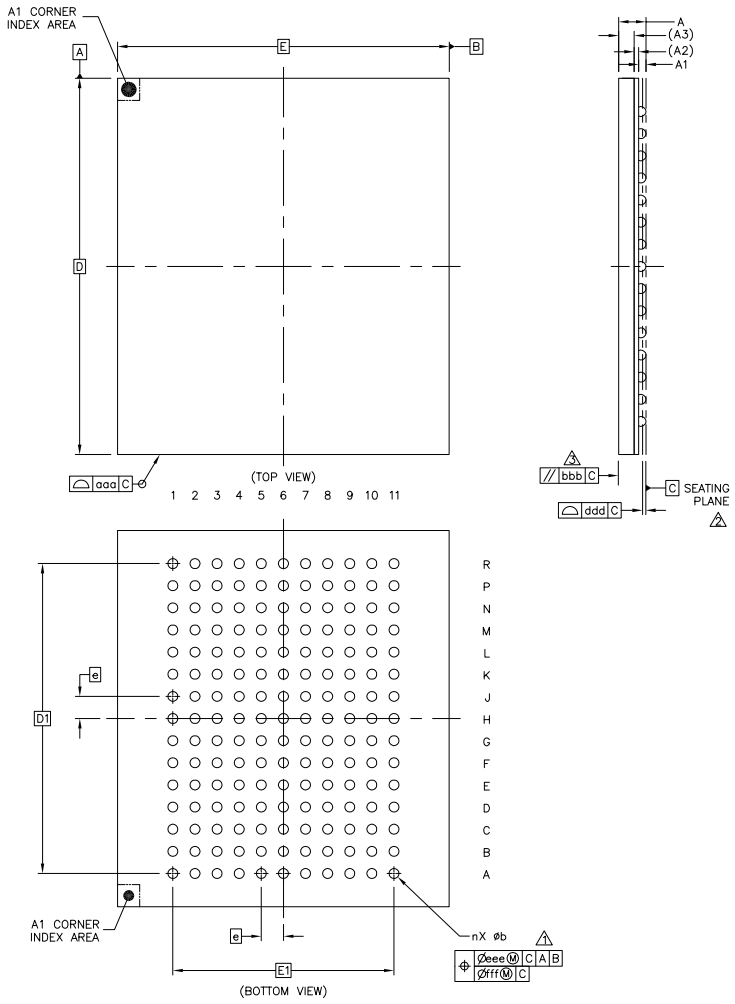
NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

Figure 13 100-pin LQFP (14 × 20 × 1.4 mm) Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.25	---	0.4
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		17	BSC
	E		15	BSC
BALL DIAMETER			0.45	
BALL OPENING			0.4	
BALL WIDTH	b	0.4	---	0.5
BALL PITCH	e		1	BSC
BALL COUNT	n		165	
EDGE BALL CENTER TO CENTER	D1		14	BSC
	E1		10	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 14 165-ball FBGA (15 × 17 × 1.40 mm) (0.45 Ball Diameter) Package Outline

Acronyms

Acronym	Description
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CE	Chip Enable
CKE	Clock Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
NoBL	No Bus Latency
OE	Output Enable
XRAM	X-Type Random Access Memory
TCK	Test Clock
TDI	Test Data Input
TMS	Test Mode Select
TDO	Test Data Output
LQFP	Low Profile Quad Flat Package
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document Revision History

Date	Version	Changes
Jan 10, 2019	Rev. A1	New datasheet